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A Review of CMOS Dynamic Power Consumption Optimization and Design Methods

Yiran Chen

School of Integrated Circuits, Shandong University, Jinan, Shandong, 250101, China

ABSTRACT
As integrated circuit processes enter the sub-nanometer era, dynamic power optimization becomes a core challenge for improving chip energy efficiency. This paper systematically examines the generation mechanism of dynamic power consumption and multi-level optimization strategies, and highlights the importance of cross-level collaborative design in breaking through the bottleneck of traditional single-level optimization. The research shows that through collaborative innovation in circuit design, system architecture and new device structure, power consumption can be significantly reduced and energy efficiency improved. The new device technology can effectively alleviate leakage problems by enhancing gate control capabilities, but its process complexity and parasitic effects still need further exploration. Future research needs to integrate material innovation, dynamic and static power management, and intelligent optimization algorithms to meet the demands of high-performance computing and the Internet of Things for low-power design.

KEYWORDS
CMOS dynamic power consumption; Power optimization; FinFET; Clock gating; Tunneling devices

1 Introduction

With CMOS process size shrinking and the exponential increase in the complexity of integrated circuits, power consumption has become a core challenge restricting chip performance and energy efficiency. Among them, dynamic power consumption, which is a direct product of the charge and discharge of the load capacitor during the transistor switching process, accounts for more than 60 percent of total power consumption. Its optimization is of great significance for improving chip energy efficiency and reducing heat dissipation requirements. Since the birth of CMOS technology, dynamic power optimization has always been closely associated with process evolution and design method innovation. Early research focused on circuit-level technologies such as clock gating and voltage regulation, but as the process moved into sub-10-nanometer nodes, leakage problems caused by short-channel effects intensified, making the trade-off between dynamic and static power consumption a new challenge. Meanwhile, the demanding requirements for energy efficiency in applications such as high-performance computing and the Internet of Things have further driven the exploration of cross-level collaborative optimization and new device architectures.

Significant progress has been made in the field of dynamic power optimization in recent years. At the circuit level, technologies such as clock gating and dynamic voltage-frequency modulation (DVFS) have achieved 20% to 30% reduction in power consumption [1]; At the system architecture level, approximate computing and dynamic thermal management (DTM) technologies have further tapped into energy efficiency potential [2]; At the process level, power consumption is reduced by 10%-30% through wiring adjustments and ΔΣ modulator technology [3]. However, most of the existing technologies are limited to single-level optimization and face a comprehensive trade-off bottleneck.

This paper systematically reviews the generation mechanism, optimization methods and device effects of CMOS dynamic power consumption, integrating innovative techniques such as voltage domain division and risky resonance suppression. The dynamic power regulation mechanism of devices such as FinFET is analyzed, and a cross-level collaborative design method is proposed.

2 CMOS dynamic power generation mechanism

The CMOS dynamic power generation mechanism is mainly derived from the signal switching process when the logic circuit is working, and its core consists of three parts. The first type is AC switching power, which is caused by periodic charging and discharging of the load capacitor, and its expression is:

$$P_D = \alpha C_L f V^2{}_{dd} \tag{1}$$

Where α represents the switching activity factor (i.e., the probability of signal flipping), C_L is the load capacitance, f is the operating frequency, and V_{dd} is the power supply voltage. This power consumption is positively correlated with voltage

* **Corresponding Author:** 202200400078@mail.sdu.edu.cn

square, frequency and load capacitance, and is the dominant factor of dynamic power consumption [4-5].

The second type is the DC switching power (short-circuit power). When the CMOS logic gate is not ideally switched on the input signal (such as when there is a transition interval between the rising edge and the falling edge), the PMOS and NMOS transistors will briefly conduct simultaneously, forming a direct path current from the power supply to ground. The power consumption can be expressed as:

$$P_L = V_{dd} I_{sc} \tag{2}$$

Where I_{sc} is the short-circuit current intensity [6]. In addition, the optimization of dynamic power consumption focuses on reducing the power supply voltage, reducing the load capacitance (through process optimization or physical design), and reducing the signal reversal rate (such as using gray code, gated clock technology), which requires collaborative design at the system architecture and circuit levels [4-5].

3 Dynamic power consumption optimization methods

3.1 Voltage optimization with load capacitance

Voltage domain division reduces global power consumption by dividing the system into high, medium and low voltage sub-modules (for example, the storage module adopts high voltage and the peripheral devices adopt low voltage), combined with level conversion technology [8]. Dynamic Voltage scaling (DVS) technology further adjusts the voltage and frequency according to the real-time load of the module. Experiments show that the CC2+ clock gating condition can significantly reduce the total power consumption of the general-purpose CPU [9]. The load capacitance needs to take into account both the device gate capacitance and the interconnect capacitance. Shortening the line length during the layout and routing stage, using small transistors and low-capacitance logic units can significantly reduce the total capacitance. It is worth noting that in advanced processes, interconnect capacitors account for more than device capacitors, making the optimization of interconnect design crucial [7].

3.2 Clock gating technology and signal integrity

Clock gating technology effectively reduces invalid flipping by enabling signals to shield the clock allocation of inactive modules. Latch-based gating techniques can reduce dynamic power consumption and avoid glitter interference, and experiments have shown that they outperform flip-flop schemes. Advanced clock gating technology reduces the number of redundant pulses by predicting clock requirements in advance, making it suitable for scenarios with high timing constraints. In addition, glitches occur due to differences in combinational logic path delays, and inserting buffers or registers can significantly suppress ineffective jumps [8].

3.3 Architecture-level optimization

At the architecture level, cache design needs to balance performance and energy consumption. Experiments show that when the number of blocks in the first-level data cache is increased to 2048, the instruction cycle (CPI) drops from 1.074 to 1.004, and the total energy consumption is at its lowest point under a specific configuration, with an improvement of 18%. The progress in manufacturing process has a significant impact on power consumption, with static power consumption rising to 42% in the 90nm process and dynamic power consumption decreasing by about 50% as the voltage drops [9]. To address leakage issues, multi-threshold voltage technology has been widely adopted to reduce static power consumption without sacrificing performance [7]. In addition, power gating technology cuts off the power supply of inactive modules through a gate control, reducing the leakage current in the off state to less than 10 percent of the operating state [9].

3.4 Risky Resonance with maximum power suppression

Multi-functional modules (such as adders, multipliers) are prone to trigger risky resonance when data bus synchronization jumps, resulting in a sudden surge in power consumption. By simplifying the 8-bit bus to single-line control, the maximum power search space can be compressed, significantly improving estimation efficiency [9]. Further, bus coding techniques, such as Gray code, reduce bus-related power consumption by reducing the number of jumps in adjacent data transmissions [7]. The genetic algorithm combined with the application of the delay model optimizes the power-on current estimation, and the maximum current under the fan-out delay model is 2.1 times higher than that under the delay-free model, verifying the actual impact of the risk-taking phenomenon [9].

4 The effect of device structure on dynamic power consumption

4.1 Dynamic power consumption bottleneck of traditional MOSFETs

At sub-10-nanometer process nodes, traditional CMOS inverters face the problem of leak-induced barrier reduction caused by short-channel effects, resulting in a significant increase in static power consumption. Although dynamic power still dominates, the growth trend of static power reveals the urgency of dynamic power optimization. The switching power consumption of conventional planar MOSFETs is difficult to be effectively reduced because the threshold voltage and power supply voltage cannot be reduced proportionally with process size [10,13].

4.2 Performance analysis of FinFET and GAA structures

FinFET enhances gate control capability through a three-dimensional gate structure, significantly reduces off-state current compared to traditional planar MOSFETs, and effectively improves dynamic power consumption. However, the complexity of the three-dimensional structure leads to a decline in manufacturing yield and may introduce additional parasitic capacitance, partially offsetting the dynamic power optimization effect [10,13]. The encirclement gate (GAA) structure, with a fully encirclement gate design, further optimizes subthreshold swing and leakage current levels, showing better potential for dynamic power control than FinFET [13]. Specific experimental data show that the hybrid logic design based on FinFET split-gate devices can reduce dynamic power consumption by 9.4% to 41.4%, mainly due to the reduction in the number of transistors and parasitic capacitance [14].

4.3 Dynamic power optimization of the new device structure

4.3.1 Innovative features of TFET devices

The three-sided tunneling dual-threshold independent gate TFET achieves dual-threshold logic functionality by increasing the tunneling contact area and enhancing the open-state current independent gate design, reducing the number of transistors. At low operating voltages, its dynamic power consumption is 8 times lower than that of conventional MOSFETs. But pay attention to the effect of increased Miller capacitance [13].

4.3.2 Hybrid structure design strategy

FinFET splitter devices have demonstrated advantages in hybrid logic designs: the number of transistors in XOR/XNOR circuits has been reduced from 10 to 5-8, the load capacitance has decreased, and the dynamic power consumption has been significantly optimized [14]. The delayed push-pull structure eliminates short-circuit current with a 5ns timing delay, reduces dynamic power consumption by 32% under a 100pF load, and drops peak current by 20%[12].

4.4 Synergistic optimization technology path

The combination of III-V group materials with the fence structure can increase the tunneling probability and increase the open-state current. [13]SOI technology reduces parasitic capacitance through oxygen layer isolation, and quantum dot devices' ability to suppress carrier scattering reduces switching power consumption. Asynchronous timing design effectively reduces redundant clock switching operations by dynamically adjusting the clock frequency [11].

5 Conclusions

This paper systematically reviews the generation mechanism, optimization methods and device structure evolution trends of CMOS dynamic power consumption, and highlights the importance of cross-level collaborative design and new device technologies. The optimization of dynamic power consumption should focus on lowering the power supply voltage, reducing the load capacitance, and suppressing the signal reversal rate. Clock gating and other technologies have achieved results in practical applications, but most of the existing technologies are limited to single-level optimization, making it difficult to achieve global optimal energy efficiency. New device architectures offer new ideas for dynamic power optimization. FinFET and GAA and other three-dimensional gate technologies significantly reduce leakage current and optimize dynamic power consumption by enhancing gate control capabilities, but their complex manufacturing processes and parasitic capacitance problems still need to be further addressed. Tunneling devices such as TFET have shown potential for reduced dynamic power consumption in low-voltage scenarios, but they are affected by Miller capacitance. Hybrid structure designs, such as delayed push-pull circuits, further enhance optimization efficiency by reducing short-circuit current and load capacitance. In addition, the synergistic technology path provides a viable

solution for cross-level regulation of dynamic power consumption. Future research should focus on the development of cross-level optimization algorithms, the deep integration of new devices and materials, and intelligent collaborative strategies for dynamic and static power consumption to address the harsh challenges of future high-performance computing and the Internet of Things.

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